



Graphene-based Nanoelectronics

**by Dr. Osama M. Nayfeh, Mr. Matthew Chin, Dr. Matthew Ervin,
Dr. James Wilson, Dr. Tony Ivanov, Dr. Robert Proie,
Dr. Barbara M. Nichols, Dr. Frank Crowne, and Dr. Stephen Kilpatrick**

**PI: Dr. Madan Dubey
Co-PIs: Dr. Raju Nambaru and Dr. Marc Ulrich**

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**Dr. Osama M. Nayfeh, Mr. Matthew Chin, Dr. Matthew Ervin,
Dr. James Wilson, Dr. Tony Ivanov, Dr. Robert Proie,
Dr. Barbara M. Nichols, Dr. Frank Crowne, and Dr. Stephen Kilpatrick
Sensors and Electron Devices Directorate, ARL**

and

**PI: Dr. Madan Dubey
Co-PIs: Dr. Raju Nambaru and Dr. Marc Ulrich
Sensors and Electron Devices Directorate, ARL**

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14. ABSTRACT A large program in graphene-based nanoelectronics has been initiated at the U.S. Army Research Laboratory (ARL) under the auspices of the ARL Director's Strategic Initiative (DSI). An array of capabilities for graphene growth, characterization, device fabrication, and device modeling has been established, and expertise has been gained in all facets of the research. Significant results have been achieved, including the world's highest reported f_T for a graphene field-effect transistor (GFET) fabricated from chemical vapor deposition (CVD)-grown graphene; and a first-generation graphene-based supercapacitor. This research could potentially have enormous benefits for the American Soldier including smaller and more efficient power electronics and communication systems, transparent and flexible electronics, and wearable electronics.					
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1. Introduction

Electronic phenomena in nanoscale structures have generated new challenges and opportunities for enabling new technologies never before realized. Recently, graphene has emerged as a novel material, especially for electronics, that could lead to devices in the quantum domain at room temperature (1–5). More generally, graphene represents a conceptually new class of materials that are only one atom thick (equivalent to 0.36 nm for graphene) (6), and which thus exhibit startlingly different phenomena from their traditional three-dimensional (3-D) analogs and which potentially offer unexplored capabilities for novel electronic devices and applications. Graphene is the name given to a flat monolayer of carbon atoms tightly packed into a two-dimensional (2-D) honeycomb lattice, first isolated in 2004, and illustrated schematically in figure 1. It is the basic building block for graphitic materials of all other dimensionalities and can be wrapped up into zero-dimensional (0-D) fullerenes, rolled into one-dimensional (1-D) nanotubes, or stacked into 3-D graphite.

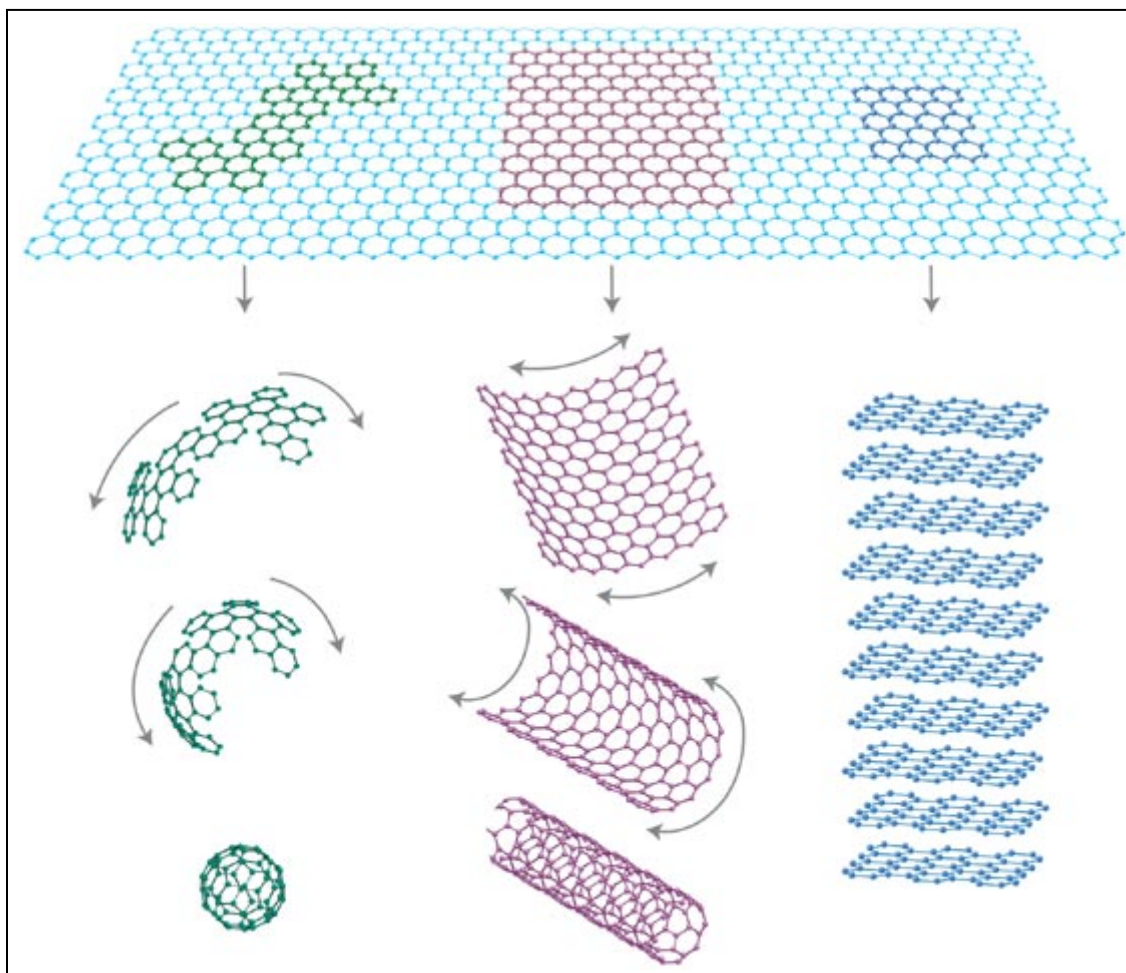


Figure 1. Graphene is a 2-D building material for graphitic materials of all other dimensionalities. It can be wrapped up into 0-D buckyballs, rolled into 1-D nanotubes, or stacked into 3-D graphite (1).

Graphene possesses a high electron and hole mobility with values shown as high as $200,000 \text{ cm}^2/\text{V-s}$ (7), a high thermal conductivity of $\sim 5 \times 10^3 \text{ W/m-K}$ (8), temperature stability to at least 2300°C (but only $\sim 500^\circ\text{C}$ in air [9]), extremely high tensile strength measured to be 1 TPa (10), quintessential flexibility, stretchability to 20% (11), a high breakdown current density exceeding 10^8 A/cm^2 (12), and superior radiation hardness (13). All of these qualities are desired in electronic materials. In addition to these advantageous characteristics, graphene also possesses very unique ambipolar properties (capable of conducting electrons when biased one direction and holes when biased in the other direction) that open up a whole new class of electronic devices.

Graphene lacks a bandgap in its energy band diagram, and therefore, exhibits metallic conductivity even in the limit of nominally zero carrier concentration. At the same time, most electronic applications rely on the presence of a gap between the valence and conduction bands. Several routes have been reported to induce and control such a gap in graphene. Some examples include using the effect of confined geometries such as quantum dots or nanoribbons, doping the

edge states or the bulk of the graphene, applying a transverse electric field to a bilayer of graphene (14), and exploiting the proximity effects from an adjacent substrate or insulator layer. Current research shows that graphene's atomic interaction with an epitaxial silicon carbide (SiC) substrate can induce a splitting of up to 0.3 eV between the maximum of the valence and minimum of the conduction bands at the Dirac-point (15).

We at the U.S. Army Research Laboratory (ARL) are harnessing the electronic properties of this newly discovered material, finding ways to develop and exploit a new generation of electronic and sensor devices for Army-specific applications. While many in the field are exfoliating micron-sized sections of graphene from chunks of graphite to study its fundamental physics or for measurements of unipolar complementary metal-oxide-semiconductor (CMOS)-like devices to extend Moore's Law, our approach is to synthesize our graphene using a manufacturable process, i.e., by chemical vapor deposition (CVD), and to study a new class of graphene devices and circuits that harness the unique ambipolar properties of graphene. Such ambipolar devices and circuits hold the promise of more efficient and smaller analog circuits, increased frequency ranges, lower power consumption, and higher data transmission speeds, all in a transparent/invisible/durable/flexible form factor. This latter attribute could lead to wearable electronics woven into a Soldier's uniform (so-called electronic textiles or "e-textiles"), for instance for wireless communications or to sense health and medical condition. Medical sensors using graphene-based e-textiles, in turn, could be used to wirelessly transmit information to a central command node, trigger automated drug delivery (e.g., insulin), or be incorporated within "smart bandages," which could accelerate healing of wounds. Many of the military advantages listed above could be also transitioned to civilian and commercial usages, which could make a large impact on the day-to-day world in which we live.

Further, as more sophisticated electronics are deployed to the battlefield, energy requirements become a greater burden to the Soldier. Exploiting the unique properties of graphene, we are pursuing two avenues for solutions. First, as we have said, we are developing a new class of graphene-based nanoelectronic technology that would potentially replace larger, heavier, and power-hungry components in communications systems and portable electronics. Second, we are developing a new type of energy storage device called a supercapacitor, which uses graphene or carbon nanotubes (CNTs) and an electrolyte to produce ~100 times the specific power of batteries and fuel cells. Supercapacitors are capable of millions of charge/discharge cycles, rapid charge and discharge times, and high efficiencies. This research, in collaboration with Communications-Electronics Research Development and Engineering Center (CERDEC), aims to create a printable capacitor monolithically integrated with printable electronics to produce power for integrated electronic and sensor circuits.

In this first year of research under the ARL Director's Strategic Initiative (DSI) program, we have focused on developing in-house capabilities and infrastructures for producing electronic-grade graphene, characterizing its properties by a number of metrology tools, fabricating graphene test structures and graphene field-effect transistors (GFETs) incorporating a large

variety of dielectric materials, testing these electronic structures and devices at DC to RF frequencies, exploring the use of graphene in supercapacitor devices for energy storage, and initiating efforts to model and simulate graphene device performance. Accordingly, the rest of this report is divided into the following sections: section 2: Graphene Growth and Characterization; section: Radio Frequency (RF) Top-Gated CVD Field-effect Transistors (FETs); section 4: Carbon Nanotube/Graphene Supercapacitors; section 5: Simulation and Modeling; and section 6: Conclusions.

Early on in our program, we identified two universities that were executing strong programs on graphene and that had established capabilities and directions that were well aligned with our own goals. The first is the Massachusetts Institute of Technology (MIT)—Profs. Palacios (*16*), Kong (*17*), Jarillo-Herrero (*18*), and Dresselhaus (*19*)), with significant progress in graphene-based ambipolar devices and circuits, as well as in graphene growth by CVD and the production of suitable starting structures for device fabrication. The second is Rice University—Prof. Ajayan (*20*), who has made exciting progress on some key building blocks for high performance graphene electronics, such as the co-synthesis of graphene with boron nitride (another purely 2-D monolayer and an excellent dielectric material for advanced GFET devices), and the discovery of how to make graphene repetitively reconfigurable between semiconducting and insulating states. Collaborative arrangements have been established with both of these institutions in order to enhance our efforts, and these are reflected in the report.

2. Graphene Growth and Characterization

2.1 Chemical Vapor Deposition Furnaces

The capability to produce graphene thin films in-house at ARL is important to the success of the DSI. Epitaxial graphene growth on SiC has been the primary graphene growth technique for over five years; however, in recent years, CVD of graphene on metal substrates has shown great promise. CVD offers lower processing temperatures and cheaper substrate materials, and is considerably less difficult to set up in a laboratory setting than a high temperature furnace for graphene growth on SiC.

Two CVD furnaces were established for in-house graphene growth: an atmospheric pressure chemical vapor deposition (APCVD) furnace and a low pressure chemical vapor deposition (LPCVD) furnace. APCVD graphene growth was performed in the existing CNT furnace. Growth conditions for CNTs and graphene are very similar. Both use the same process gases: argon (Ar), hydrogen (H₂), and methane (CH₄). The major differences between CNT and graphene growth are the substrate materials and the gas flows. As reported in the literature, CVD growth of single layer and bilayer graphene takes place at low methane flow rates (typically, 3–10 sccm) (*21, 22*). In order to accommodate the smaller flow rates, a new methane

mass flow controller (MFC) was purchased and installed. The APCVD furnace was primarily used to grow graphene on nickel (Ni) thin films.

A new LPCVD furnace system was constructed at the Adelphi Laboratory Center (ALC), MD, this year. In hindsight, the purchase of a commercially established growth system may have been a prudent, albeit more costly, approach. It has been shown that single layer graphene, while difficult to produce using APCVD, can be produced under low pressure on copper (Cu) foils (23, 24). The key components to the system are the (1) gas delivery/handling system, (2) furnace, and (3) exhaust system. Located adjacent to the APCVD system, the LPCVD system is plumbed with the same gases as the APCVD system: hydrogen, nitrogen, argon, methane, ethylene, and compressed air. The flammable gas flows are regulated using MFCs, while rotameters are used for the inert gases. The flammable and inert gases are kept in separate manifolds until they are mixed right before entering the furnace. All valves on the system are pneumatically controlled and switched manually by an electronics panel. Once the gases reach the furnace, the gases enter a 2-in quartz tube heated by the furnace. The furnace can reach a maximum temperature of 1200 °C; however, it is typically operated at lower temperatures. The quartz tube and piping are evacuated by a mechanical roughing pump. A baratron gauge downstream of the furnace measures the system pressure, and a butterfly throttle valve can be operated to set and control the pressure. The system can reach pressures as low as 250 mTorr. The LPCVD furnace has primarily been used for graphene growth on Cu foils.

2.2 Growth on Copper

The growth of graphene on Cu foils was demonstrated in the new LPCVD system. Cu foils (Alfa Aesar #13382, 99.8% Cu, 0.025 mm thick) were cut to approximately 1- x 1.5-in strips and cleaned using the following procedure: acetone rinse, water (H₂O) rinse, soak in glacial acetic acid for 10 min, followed by a quick rinse in acetone, isopropanol (IPA), and then blow-dried with nitrogen.

Once the foils are loaded onto a boat and inserted in the furnace, a four-step growth process is initiated. There are four distinct steps for the growth process: a ramp-up stage, a 30-min annealing stage, a 40-min growth stage, and a cool down period (figure 2). During the ramp-up stage, the first 25 min of the anneal stage, and the cool down period, the pressure remains at 0.5–0.7 Torr; however, the growth stage pressure was held constant at 1.5 Torr. Hydrogen was flowed at a steady rate throughout the process; methane was only added during the “growth” stage. The gas flow rates for the hydrogen and methane were varied to determine the optimized growth conditions for producing single layer graphene.

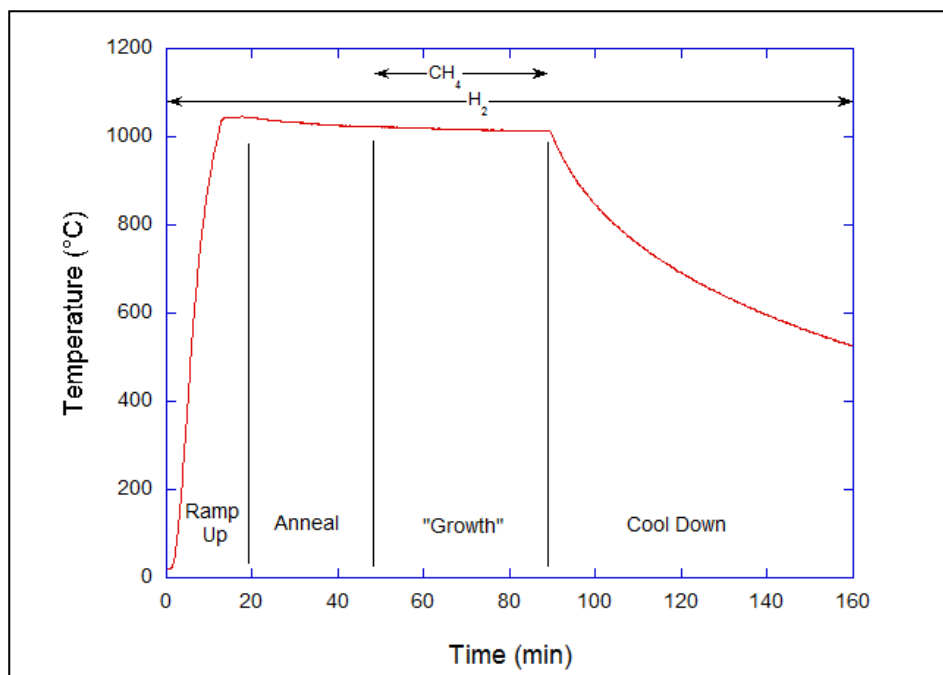


Figure 2. Four-step process for graphene growth on Cu foils.

Once deposited, a graphene transfer process was employed to separate the graphene layer from the Cu foil and to place the graphene onto an oxidized silicon (Si) substrate (see figure 3). To begin this process, a protective bilayer of poly(methyl methacrylate) (PMMA) was spun onto one side of the Cu foil and baked on a hot plate. Next, the unprotected backside graphene layer was removed using an oxygen plasma etch. The Cu foil was then etched away by floating the sample with the PMMA-coated side up in Cu etchant for approximately 1 h. Following this, the PMMA/graphene were rinsed with water and placed in a 10% hydrochloric acid/water solution for 1 hr. The samples were then rinsed in water, transferred onto the silicon dioxide (SiO₂) substrate, and nitrogen blow-dried. The PMMA bilayer is either removed in an acetone vaporization process or annealed in an atmospheric pressure furnace. It was later found that removal of the PMMA layers could be very challenging. The acetone vaporization procedure can mechanically damage the graphene material, causing it to split. The preferred removal method is thermal annealing; however, there exists a potential to graphitize the PMMA layers and leave a carbonaceous residue on the surface.

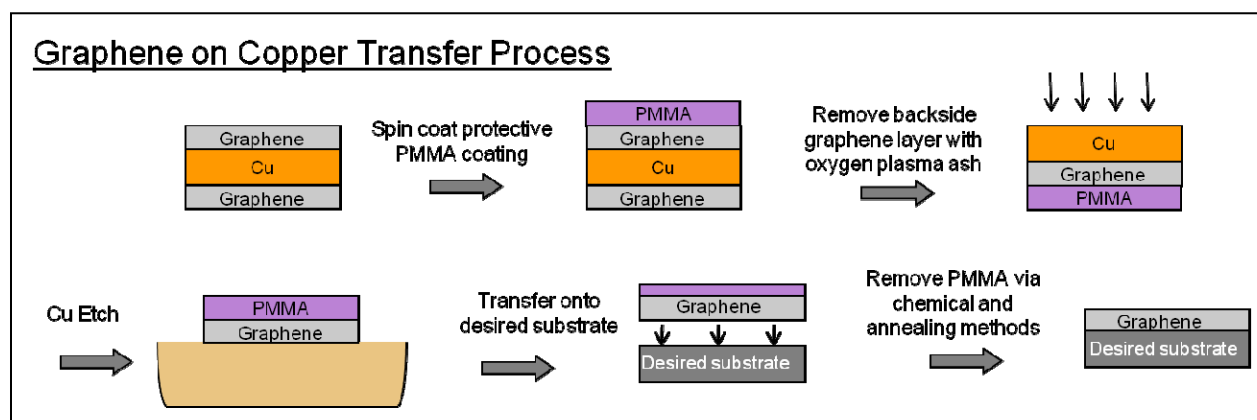


Figure 3. Transfer process of graphene grown on Cu foils to desired substrate.

2.3 Growth on Nickel

More than 100 graphene samples have been grown on Ni thin films using the APCVD furnace described previously. Ni catalyst layers were first created on 4-in thermally oxidized Si wafers (usually 300 nm of SiO₂) using electron beam deposition. Generally, these were 300-nm Ni thin films with an underlying 30-nm adhesion layer of chromium (Cr). For a graphene synthesis run, samples approximately 13 mm² were cleaved from the Ni-coated wafers and soaked in acetone for 10 min, followed by 10 min in IPA and blown dry in N₂.

Once samples were arranged on a quartz boat and loaded into the CVD furnace, a four-step procedure was carried out to produce layers of graphene, similar to the process described previously for growing on Cu. In the ramp-up and Ni-anneal stages, a mixture of H₂ and Ar was passed through the furnace. The 20-min annealing to remove any Ni oxides and improve the Ni microstructure by enlarging the crystalline grains was generally conducted at 1000 °C. In the third stage, a small amount of CH₄ was added to the gas stream, which dissociated in contact with the Ni catalyst. The resulting carbon atoms promptly diffused into the Ni layer, while the H₂ returned to the gas phase. Once enough carbon had entered the Ni lattice (generally 10 min), the furnace temperature was slowly decreased in the ramp-down stage, while still maintaining the CH₄ flow. As the sample temperature decreased, the solid solubility limit (the maximum atomic fraction allowed by thermodynamics) for carbon in the polycrystalline Ni decreased substantially, and the excess carbon which was no longer allowed in the Ni was expelled to the surface, and self-assembled to form graphene. Multiple layers of graphene are possible by this approach, so the amount of carbon first placed in the Ni thin film must be tightly controlled. Carbon precipitates more readily at the Ni grain boundaries, leading to excess layers of graphene at those locations. The graphene film can be removed from the Ni and transferred to an arbitrary substrate using a process similar to that shown in figure 3.

Figure 4 shows a typical optical microscopy image of graphene on Ni after growth. The puckered surface topology of the Ni grains is quite evident. The dark irregular patches are regions of multilayer graphene (MLG), with the level of darkness corresponding closely to the

number of layers. The remainder of the sample, which has the lightest shading, is largely covered by 1–2 monolayers of graphene as determined by Raman spectroscopy (see figure 4), which is considered best suited for electronic device fabrication. Since one approach to creating an electronic bandgap in graphene is by applying a transverse electric field to a graphene bilayer, and growth of graphene on Ni lends itself to the growth of more than one layer, this synthesis route may be a valuable one for our future research.

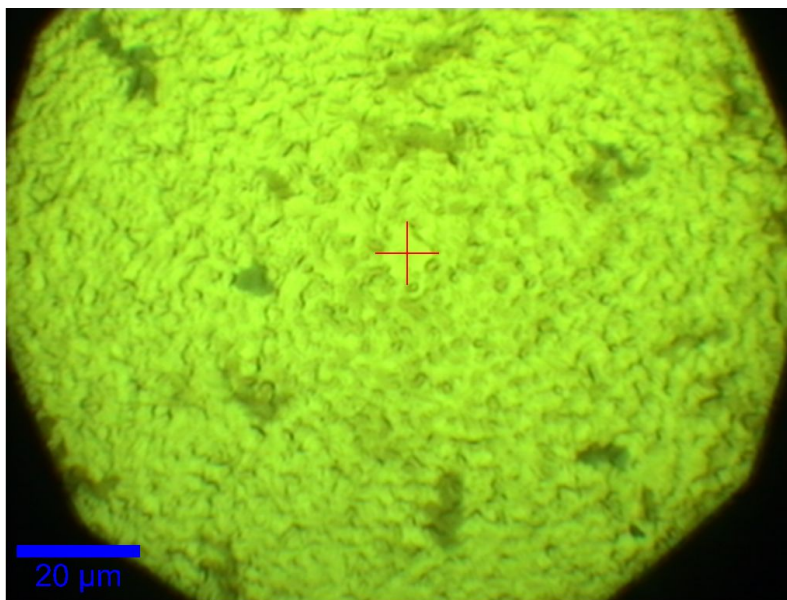


Figure 4. Optical microscopy image of graphene on Ni. The dark irregular patches are extra layers of graphene typically located at Ni grain boundaries (not visible).

2.4 Characterization by Raman Spectroscopy

Raman spectroscopy has proven to be a powerful yet relatively simple and nondestructive characterization tool for graphene. Raman measurements were performed on a Renishaw inVia microscope system at 514 nm (spot size $\sim 1 \mu\text{m}$, 1800 lines/mm grating). The characteristic peaks for graphene are the D, G, and 2D, located at $\sim 1350 \text{ cm}^{-1}$, $\sim 1580 \text{ cm}^{-1}$, and $\sim 2700 \text{ cm}^{-1}$, respectively. The G band arises due to the C–C bond in graphitic materials and can be found in all sp^2 bonded carbon materials. The 2D band, also known as the G' band, results from a double resonance or second-order scattering process and is sensitive to the number of graphene layers present. The presence of disorder in the sp^2 carbon materials is detected by the D band. The peak position, shape, full-width-at-half-maximum (FWHM), and intensity ratios of the different bands indicate the film quality level as well as the number of graphene layers.

An optical image of a transferred graphene film grown on Cu and the Raman spectra from various points in the image are shown in figure 5. There are several significant features from Raman data that can be discussed. First, the 2D band intensity is much greater than the G band peak for all five points shown. The I_{2D}/I_G ratio for the five points averages 2.33. Secondly, the

FWHM values for the 2D band vary between 35 and 38 cm^{-1} . It is typically known that I_{2D}/I_G values >2 are indicative of monolayer graphene, and the 2D FWHM of single layer graphene (SLG) has been reported to range between 30 and 35 cm^{-1} . The I_D/I_G ratio for the points shown ranged between 0.13 and 0.22, considered to indicate a relatively low defect density in the material. These results are in good agreement with previous studies of CVD graphene on Cu (23–25). Additionally, the Raman data shows that there is good uniformity of monolayer graphene across the sample.

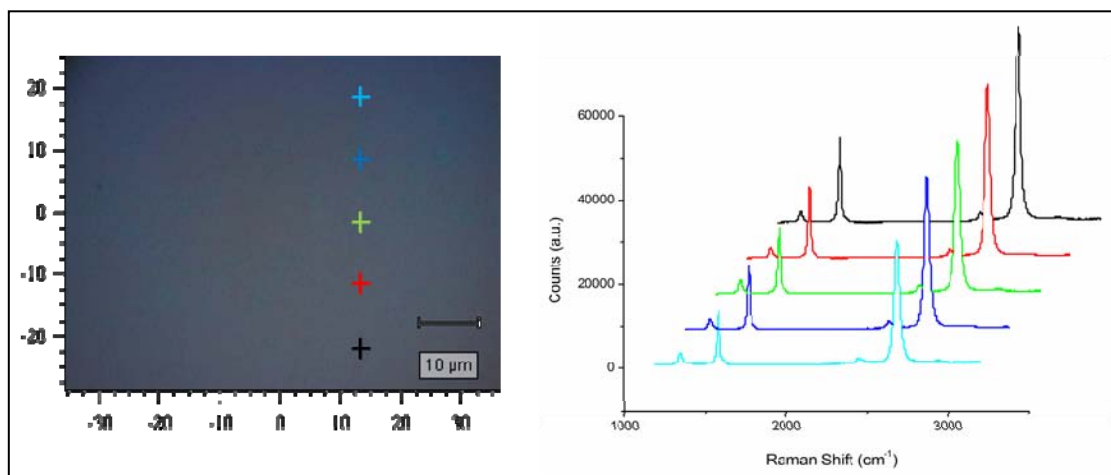


Figure 5. Raman spectra from a transferred graphene film: (a) optical image of a transferred graphene film originally grown on copper, and (b) the Raman spectra from five points on the image. The colored crosses on the optical image correspond to the colored Raman spectra taken at the respective points.

2.5 Graphene Exfoliation

2.5.1 Overview and Purpose

Methods for synthesizing graphene are necessary to keep an in-house supply available for device fabrication and material characterization. Based on the technique first developed by Geim and Novoselov (26) in 2004, the process of mechanical exfoliation (also referred to as the “Scotch tape method”) involves the use of an adhesive tape to strip single- and few-layer sheets of graphene from a highly ordered pyrolytic graphite (HOPG) source. The resulting graphene extracted via this method tends to produce, high quality, well-ordered, uniform graphene areas on arbitrary substrates. In the case of bilayer or few-layer graphene, A-B stacking tends to be the typical layer-to-layer alignment.

While ARL has the infrastructure and capability to grow graphene on metal catalysts using APCVD and LPCVD, exfoliated graphene provides a reference material due to the fact that it is the most common method for acquiring graphene and is commonly used in university laboratories. As such, most research groups using graphene provide results based on exfoliated graphene. It also provides a high quality reference material with few defects to compare with the graphene grown using CVD-based processing. If necessary, this material can be used for graphene device fabrication.

2.5.2 Process Description

The process used for mechanical exfoliation at ARL is based on the process developed at MIT by Prof. Pablo Jarillo-Herrero's group. Si wafers with 300 nm of thermally grown SiO_2 are cleaned and prepared as the final substrate for the exfoliated graphene. Specialized graphite flakes purchased from NGS Naturgraphit GmbH were exfoliated using the 1007R6 adhesive film from Ultron Systems. A graphite flake was placed on the adhesive film, which was then folded and pulled apart repeatedly until the graphite flake was thinned down to roughly a few graphene layers thick. The thin sheets of graphite covering the adhesive film were then gently pressed against a SiO_2/Si wafer using fluorinated plastic tweezers. Figure 6 provides images of the process step-by-step while figure 7 depicts optical micrographs of exfoliated graphene. After the removal of the adhesive film, an optical microscope was used to locate graphene areas on the sample. Once the graphene areas were located, the quality of the material and the number of layers were determined using atomic force microscopy (AFM) and Raman spectroscopy. Figure 8 presents an example of an AFM image of an area of graphene with differing numbers of layers.

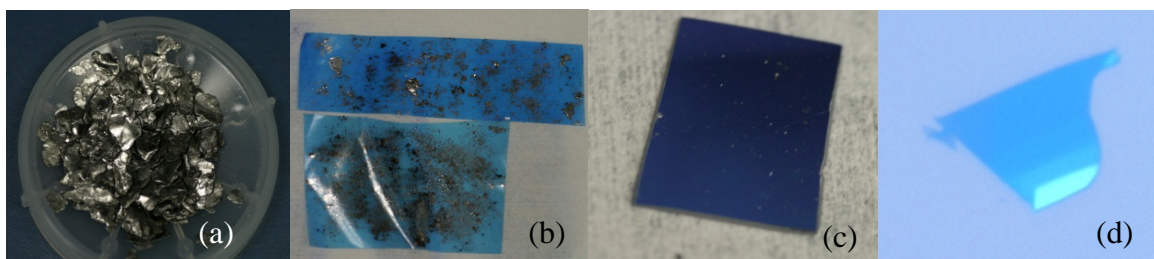


Figure 6. A pictorial of the mechanical exfoliation process. (a) Highly-oriented pyrolytic graphite flakes (“graphenium”) are used as the source material. (b) A special adhesive film in the form of tape with extremely low residue is used to split the graphite flakes along their crystal planes. This process is repeated several times until single- or few-layer graphene flakes are produced. (c) The graphene flakes are then transferred to a Si substrate with a 300-nm layer of thermally grown SiO_2 . (d) Optical microscopy is used to locate graphene areas on the substrate, and then Raman spectroscopy and AFM are used to determine the number of graphene layers and their quality.

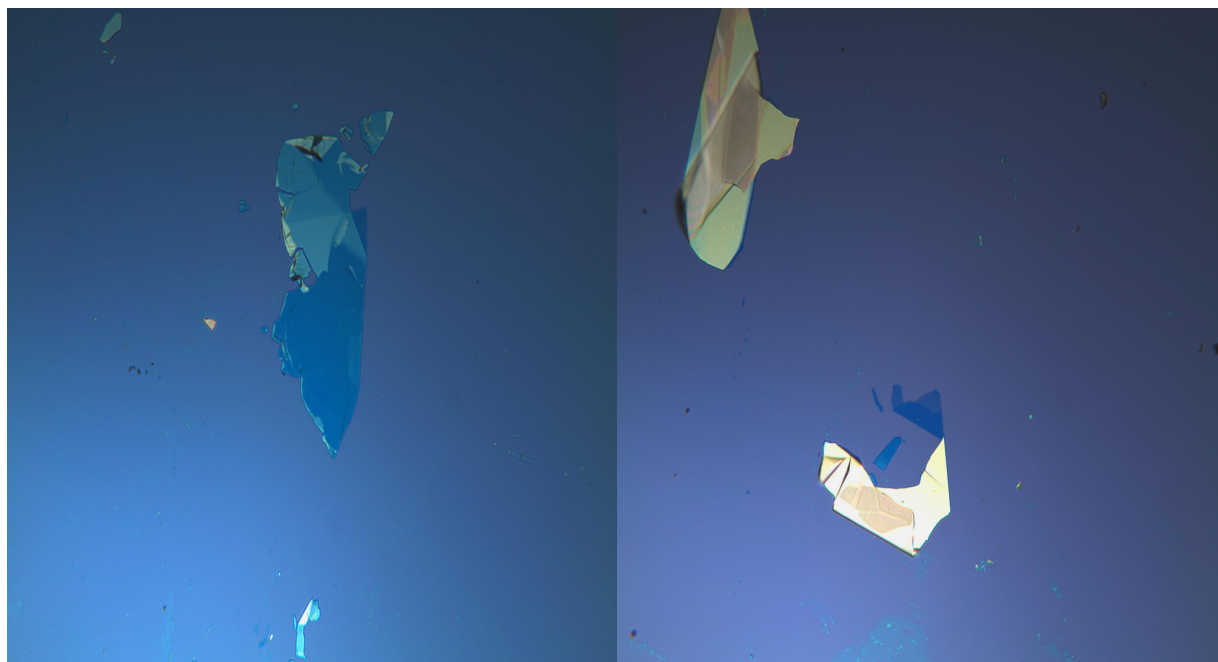


Figure 7. Optical micrographs of two areas on 300 nm of SiO₂ with graphene and graphite present. The yellow areas indicate the presence of thick, multilayer graphite, while the blue areas indicate few-layer and even monolayer graphene.

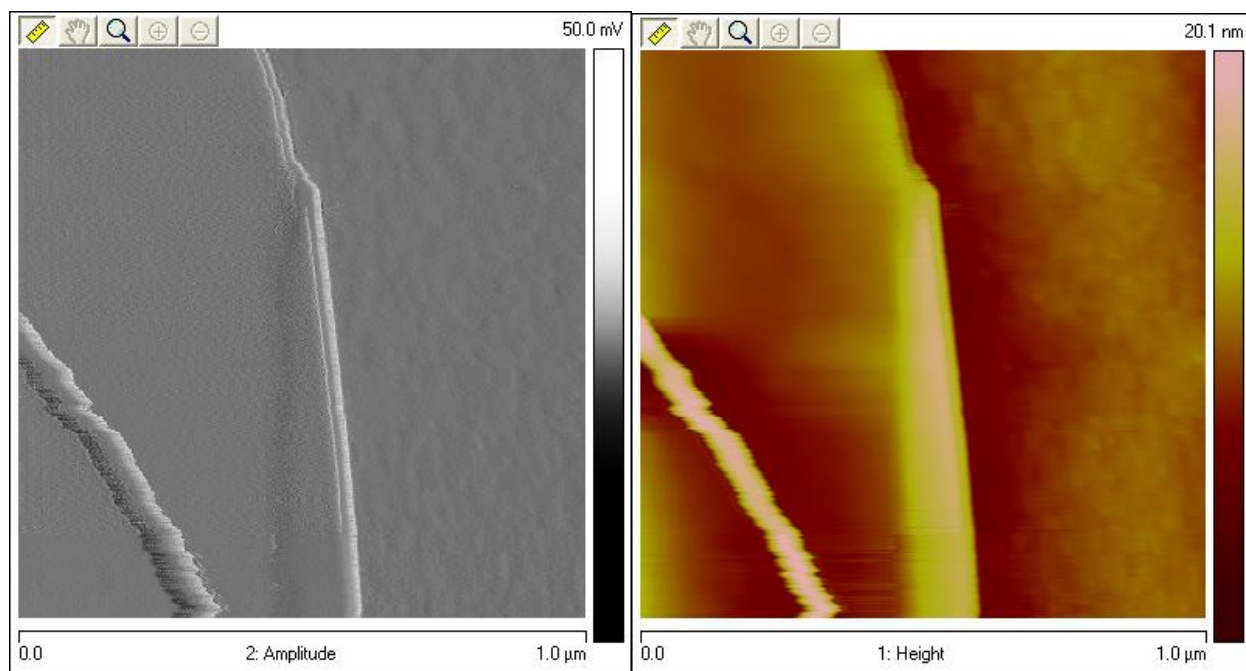


Figure 8. AFM images of mechanically exfoliated graphene at a step junction where the graphene flake transitions between differing numbers of layers.

3. Radio Frequency (RF) Top-gated CVD Graphene Transistors

3.1 Device Construction

Graphene/SiO₂/n+ Si substrates are cleaned using acetone, methanol, and IPA, followed by a de-ionized (DI) water rinse, and N₂ dry. Samples are baked on a 125 °C hot-plate for 5 min to accelerate removal of residual solvent and moisture. Source and drain contacts are formed by a lift-off process. AZ5214 photoresist is coated at 3000 rpm for 60 s and patterned to define (by image reversal lithography) source/drain contact (pad) areas. Then, 5-nm titanium (Ti)/100-nm gold (Au) is e-beam evaporated (CHA Industries). Following metal deposition, the samples are soaked for 24 h in acetone, followed by a “lift-off” procedure using subsequent rinses in acetone/methanol/IPA/H₂O. In order to minimize damage to the monolayer graphene, lift-off is not performed in the presence of ultra-sonication, and only by gentle pipette rinsing in solvent.

Following source/drain formation, active graphene channel areas are patterned with AZ5214. A gentle O₂ plasma etch (20 sccm O₂/70 W) is performed in order to define graphene channels. After definition, the photoresist is removed by soaking in acetone. Figure 9 shows an example scanning electron microscopy (SEM) image of a graphene channel region between a 5- μ m source/drain gap.

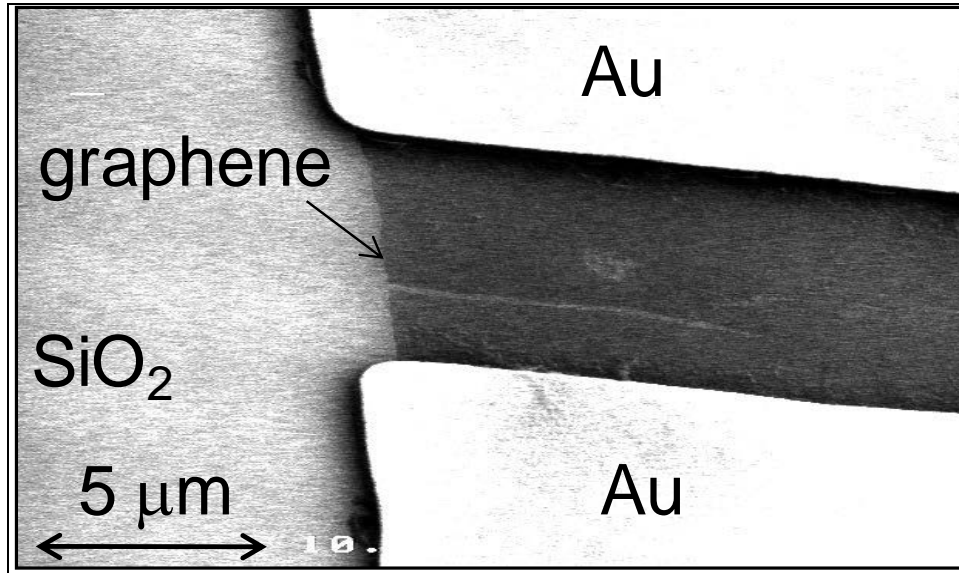


Figure 9. SEM image of a CVD graphene film between (Ti/Au) source/drain electrodes.

Prior to gate-dielectric deposition, samples are cleaned with acetone/methanol/IPA/H₂O and a 125 °C hot-plate soft-bake for 5 min. Gate-dielectric is formed by depositing by e-beam evaporation (CHA Industries) of a SiO₂ interfacial layer (9 nm), at a deposition rate of 1 Å/s,

followed by atomic layer deposition (ALD) of aluminum oxide (Al_2O_3) (15 nm). The SiO_2 also serves as a nucleation layer for the ALD dielectric as it has been shown that direct ALD deposition to graphene is difficult. Promising techniques may be possible, though it is unclear at this time what the degree of damage that may be caused and the optimal conditions for deposition. The Al_2O_3 film was deposited using alternating pulses of trimethylaluminum (TMA) and H_2O in a Cambridge Nanotech Fiji ALD system, enabled by nucleation on the SiO_2 . The thicknesses of the dielectrics were determined by spectroscopic ellipsometry measurements of films deposited with the same conditions on Si substrates and capacitance-voltage (C-V) measurements of test structures. Raman measurements were performed following gate-dielectric deposition, and an intact “monolayer” graphene layer with characteristic (graphene) peaks and only minimal increase in the level of disorder (as indicated by the so-called “D peak”) is observed. The e-beam deposition process and subsequent processing is “gentle” enough to minimize further damage and additional chemical doping of the graphene.

Top-gate metal (5 nm Ti/90 nm Au) is deposited by e-beam evaporation and lift-off (performed identical to the process for source/drain contact). The final devices have a gate-length of 3 μm with a source/drain access length (the separation distance between the gate and source/drain) of 1.5 μm .

3.2 DC and RF Performance

Electrical measurements were performed using a Keithley 4200 semiconductor characterization system. Figure 10 shows DC measurements of the drain current versus top-gate voltage (I_d vs. V_{gs}) and the transconductance vs. top-gate voltage (g_m vs. V_{gs}) with $V_{ds}=5$ V and a back-bias $V_{bs}=0$ V. The measurements show characteristic ambipolar behavior, albeit with asymmetric strengths of the electron/hole branches of the drive current. The device has a drive current of 0.5 A/mm, and a transconductance of 20 mS/mm in the hole branch under these conditions (27–28). The devices operate in a “depletion-mode,” where the Dirac point (DP) is located at ~ 5 V. It can be inferred based on the location of the DP (at positive gate voltages), that this graphene is “doped” p-type. The gate leakage in these devices with this dielectric is 2–3 orders of magnitude lower than the drain current. Using the measured g_m and C_{ox} the field-effect mobility is computed as $\mu_{FE} = (L/W) g_m / (C_{ox} \cdot V_{ds})$. The peak field-effect mobility is extracted to be 530 cm^2/Vs for the holes and 336 cm^2/Vs for the electrons. The extracted field-effect mobility for this material is lower than that typically reported for pristine exfoliated material and is likely limited by the doping levels, disorder in the film and the interactions with the external environment (including substrate).

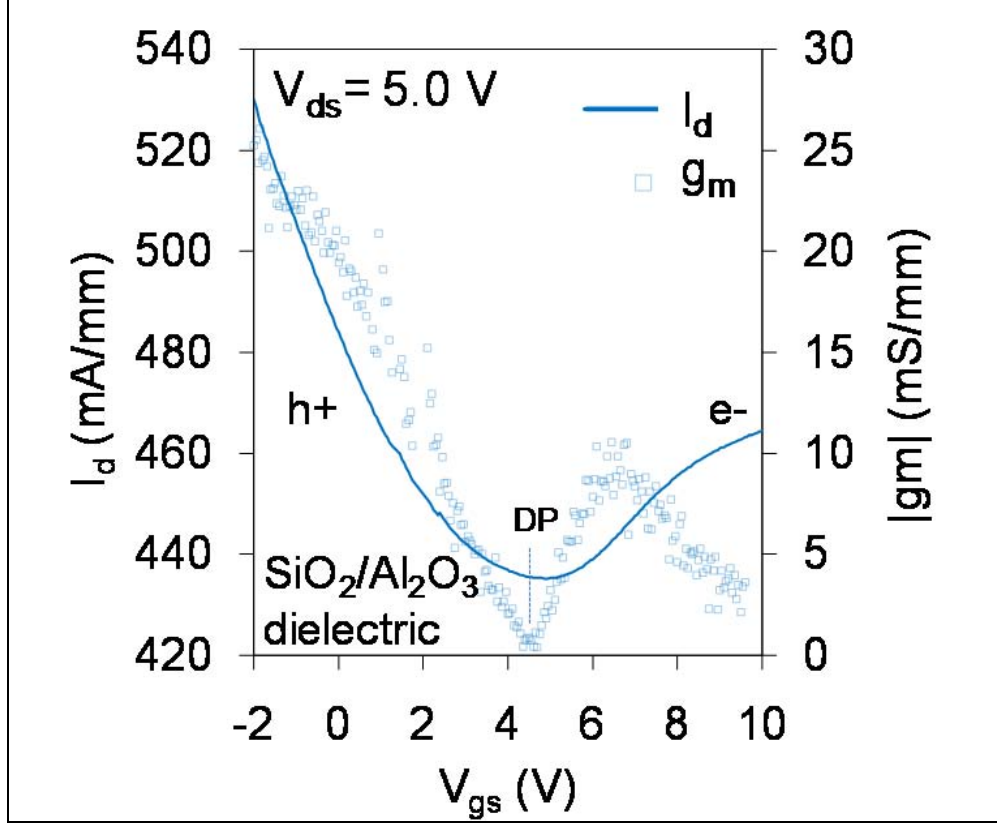


Figure 10. DC measurements (I_d vs. V_{gs}) with $V_{ds}=5$ V of a typical top-gated GFET with a gate length ($L_{gate}=3$ μm) and gate-source/drain length of 1.5 μm . The device has an ALD-based Al_2O_3 top-gate dielectric with an evaporated SiO_2 interfacial layer. The device has a peak transconductance of 20 mS/mm, drive current of 0.5 A/mm, and a location of the DP at ~ 5 V.

With $V_{gs}=0$ V, due to the p-type doping, source-drain carrier conduction is allowed by the majority carrier transport of holes in the low resistance channel. As the gate-voltage is increased, the concentration of holes in the channel is decreased (depleted) while the concentration of electrons in the (ambipolar) channel is increased until the dominant current is due to the minority carrier transport of electrons. Due to the expected bandgap of graphene (0 eV) for monolayer graphene, the transition between hole and electron dominated DC branches of current is sharp giving a small “on-to-off” ratio for the device (as observed in the DC measurements). Under conditions favorable for electron transport there exist un-gated access regions of lower electron density. Due to the presence of an intrinsic carrier density in the gapless graphene, there are enough electrons however to support current flow from source-drain.

Scattering parameters were collected via an Agilent E8361A PNA network analyzer using 125- μm pitch GSG probes. A power level of -17 dBm (~ 0.09 V_{pp}) was used to modulate the gate. Biases were supplied through the center conductor on each GSG probe via a Bias-T. Data were collected from 10 MHz to 40.0 GHz at 10-MHz steps. Figure 11 shows the measured gain (dB) versus frequency, extracted from the measured scattering (S) parameters for different values of V_{gs} , near the location of maximum transconductance, g_m (in the hole branch) with an applied

$V_{ds}=5$ V and $V_{bs}=0$ V. The measured f_T of the device is ~ 1 GHz. The measured f_T approaches that of GFETs produced recently with epitaxial graphene on SiC with a similar gate-length (29). Small signal modeling (30) based on Y parameters (converted from the measured S parameters) was performed to estimate the frequency dependence of g_m , C_{gs} , and C_{gd} . The high frequency g_m (60 mS/mm) is slightly larger than the DC g_m for the same biasing and the difference may be attributed to trap-states, which do not respond at the higher frequencies. The sheet resistance of the graphene and contact resistance of the Ti/Au contact to the graphene is measured from TLM structures to be 210 Ohms/sq and 5×10^{-5} Ohms \cdot cm². The sheet resistance is reduced from typical exfoliated graphene and is likely due to the doping of the graphene film caused by auto-doping during growth and additional doping due to the transfer process. This doping contributes to lower the access resistance of the gate-source/drain separation likely allowing for the good DC and RF performance with low back-biasing (0 V, for this case). Using $f_T = g_m / [2\pi \cdot (C_{gs} + C_{gd})]$ yields a decent agreement with the f_T from the high-frequency measurements. Optimizing and improving the graphene quality, gate-insulator and device layout; minimizing parasitics; and scaling of the devices should improve the frequency performance even further.

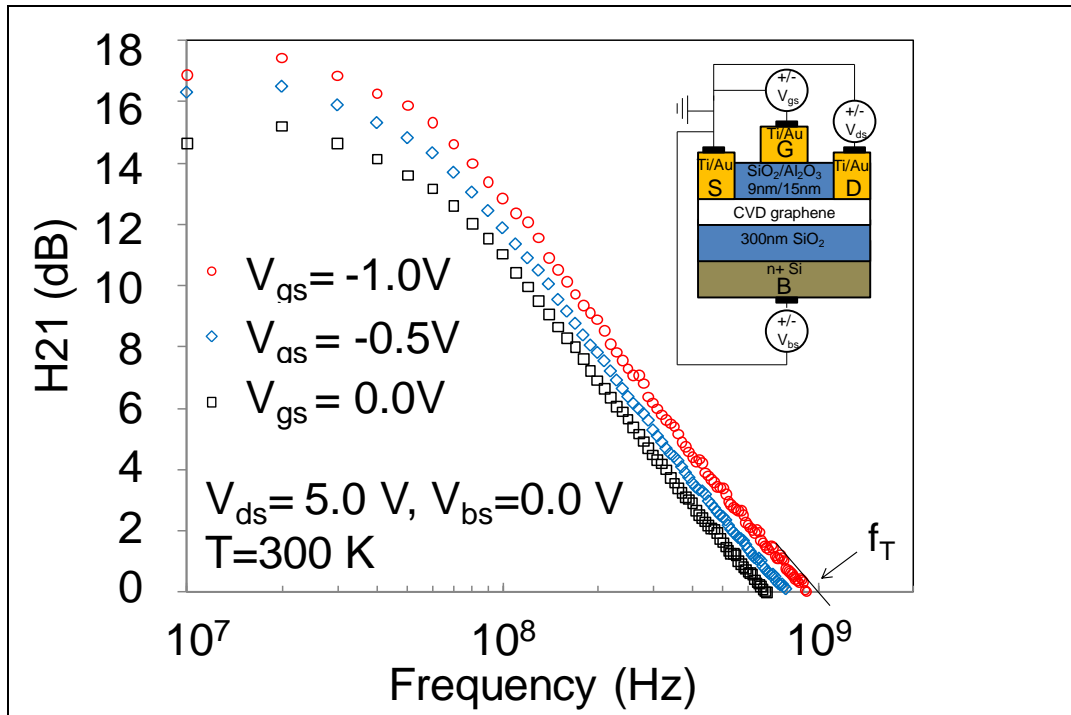


Figure 11. RF measurements (gain (dB) vs. frequency) for a typical top-gated GFET with CVD graphene channel, with a gate-length of 3 μ m and measured with increasing values of the gate-source voltage and with a $V_{ds}=5$ V and a back-bias of 0 V. A measured (extrinsic) current-gain cut-off frequency (f_T) of 1 GHz is observed for these GFET devices. This is a record frequency performance for CVD material.

4. Carbon Nanotube/Graphene Supercapacitors

4.1 Background

Supercapacitors have several advantages over conventional batteries, including higher specific power (~2 orders of magnitude higher), higher cycle life (millions of charge/discharge cycles), rapid charge/discharge times (seconds to minutes), high efficiencies (up to 98%), and unaltered performance in extreme heat and cold (31). Increasing supercapacitor energy and power densities will make them more useful for portable power applications. Carbon materials with improved surface area may increase the capacitance of supercapacitors. Two materials being studied for this are single-wall CNTs and graphene (G). Extremely large capacitances may be obtainable if these materials can be assembled in a manner that optimizes the electrode surface area that is accessible to the electrolyte.

This section details investigations into various solution-based electrode fabrication methods that are compared to determine if there is an optimum method for fabricating CNT electrodes. Solution-based fabrication of G-based flexible electrodes is also investigated. Solution-based processing was chosen as it is manufacturable and it does not impose significant thermal and chemical constraints on the underlying current collector as direct growth on the current collector would. When CNTs are deposited from solution, they typically do so in bundles. It is not yet clear if this bundling is detrimental to the resulting accessible surface area, and therefore, the resulting capacitance. In addition, the deposition method may also affect the porosity of the electrode, which will affect how easily the electrolyte ions can move into and out of the electrode (the Warburg impedance) during the charge/discharge process.

Many solution-based processing approaches have been reported, with 23–200 F/g measured, although the higher values likely include pseudocapacitive (redox reactions that behave like a capacitance) contributions (32–39). Since these papers use different CNT sources, solution compositions/processing, deposition methods, and characterization protocols, it is difficult to draw meaningful conclusions from a comparison of these works. Here we have systematically investigated the individual contributions of the solution preparation and the deposition methods.

4.2 Capacitor Evaluation

When characterizing capacitors, one needs to be careful to distinguish between true capacitance and any redox contributions. In addition, measurement methodologies can contribute to significant differences in measured capacitances. Therefore, standard test conditions of 20 mV/s have been used for cyclic voltammetry (CV) measurements made using one molar potassium hydroxide (KOH) electrolyte have been used here. To avoid inclusion of any redox contributions, the capacitance has been calculated for each electrode using the current measured at the open circuit potential on the reduction side of the CV loop. At the open circuit potential,

any reduction and oxidation reactions should be in equilibrium and make no net contribution to the measured current. Specific capacitance in Farads per gram (F/g) was calculated using only the mass and capacitance contribution of the CNTs or G. It became apparent during the experiments that there was excessive error in the measured CNT masses so the results are calculated using CNT masses based on the solution concentrations/volumes used.

4.3 CNT Solution Comparison

Both CNT and graphene materials are frequently processed as suspensions/solutions. In order to get stable dispersions, CNTs/graphene are either chemically functionalized and/or dispersed with a surfactant. Both approaches have drawbacks. Chemical functionalization can make the material more soluble, but the addition of these functional groups introduces defects that can decrease conductivity. Functional groups can also be redox active and produce undesirable decomposition byproducts over time. Surfactants can be used to solubilize CNTs or graphene, but since they are nonconductive, they typically degrade performance. Therefore, further processing is required to remove them, if possible (32).

We have made numerous electrodes using CNT solutions obtained from commercial sources. The first solutions used were of functionalized or unfunctionalized CNTs suspended in acetone using surfactants and/or dispersants. These electrodes were examined in an SEM and little porosity was seen. The anticipated porosity between the CNTs was filled with surfactant/dispersant additives. Attempts to remove these additives through thermal annealing, acid washing, or solvent extraction were largely unsuccessful. As a result, the electrodes had poor capacitances due to low accessible surface area and high resistivity due to poor tube to tube electrical contact. Subsequent electrodes were made using surfactant-free solutions of CNTs functionalized with carboxyl groups. These solutions yield much better looking and performing electrodes. It was concluded that using additive-free solutions of CNTs is the better approach even though it requires the use of less concentrated solutions. In light of these results a surfactant free graphene oxide (GO) solution has been used for fabricating our G electrodes.

4.4 Fabrication Method Comparison

At the outset of this work, it was assumed that the amount of CNT bundling would be a significant factor in the capacitance that could be achieved. It may also affect the power performance due to the electrolyte resistance to reach the interior electrode surfaces. Therefore, it was assumed that methods for producing solutions of unbundled CNTs and deposition methods that prevent re-bundling as the solution dries would be critical. We therefore selected four methods for depositing the CNT solution, which might yield different amounts of re-bundling. All four methods used a CNT solution of $\sim 70 \mu\text{g/ml}$ water without surfactants, and the current collectors were heated on a 175°C hot plate during the deposition (except for the filter and transfer method).

The simplest method, drop casting, consists of depositing droplets of solution onto the current collector and evaporating the droplets over 1–2 min with the total deposition taking about 20 min. The second method is air brushing, which sprays much smaller droplets onto the current collector which dry in 1–3 s with the total deposition time being about 30 min. The third method is filtration, which takes a few seconds, followed by transferring the dry CNT mat to the current collector by dissolving the filter paper. The last method investigated is electrospraying (40), which requires a dilution of the solution with ethanol (1:0.43 v/v water:ethanol) to decrease its surface tension. This method produces droplets, estimated to be 4 microns in diameter, which may dry before reaching the substrate. In addition, as the droplets dry in transit, they may undergo columbic explosion, which may further reduce CNT bundling.

Figure 12 shows the specific capacitances that result from these electrode fabrication methods. Focusing on the diamond symbols in the graph, which are electrodes generated with the solution used as is, it appears that these different methods do not result in greatly different capacitances. In fact, the differences may be less than they appear since the lower specific capacitances of the air brushed, filtered, and perhaps electrosprayed methods may be due to a loss of CNTs due to overspray or incomplete filtration. (Remember that the CNT masses were calculated from the solution used.) The “x” symbols in the figure represent electrodes made with sonicated CNT solution with added ethanol or water. It appears that the CNT solution dilution and sonication only results in a small difference in capacitances.

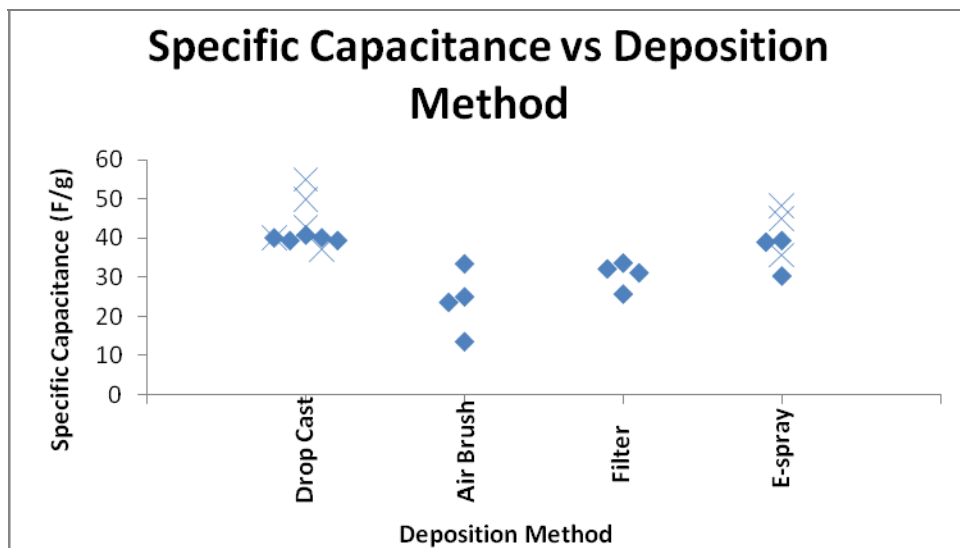


Figure 12. Specific capacitance as a function of deposition method. The diamonds are from samples made with the CNT solution merely shaken, while the “x” symbols are used to denote samples made from sonicated CNT solutions.

4.5 Flexible Capacitors

Flexible electrodes made by depositing CNTs onto paper similar to those previously reported by Hu (32) were also explored. These electrodes produced the highest specific capacitances (~100 F/g). Unfortunately, these electrodes were made using a different lot of the solution, so

direct comparisons are not quantitative. Flexible capacitors were made using these electrodes using a KOH and polyvinyl alcohol (PVA) gel electrolyte and sealing in a plastic film package. Unfortunately, the thermally sealed plastic film did not provide an adequate hermetic seal to keep the electrolyte from drying out over time. However, one interesting conclusion from this work was that infusing the electrodes with the electrolyte appeared to decrease capacitance, presumably due to the PVA blocking surface sites on the electrodes. Pressing the gel electrolyte between paper electrodes worked better. Apparently the electrodes were able to draw enough KOH solution out of the gel to wet the electrodes more sufficiently with KOH. On the other hand, the infused electrolyte electrodes produced more consistent capacitance as the electrodes were bent, due to more consistent electrode/electrolyte contact.

4.6 Graphene Capacitors

Graphene-based capacitors have been fabricated predominantly using a drop casting or dip coating method. This work has focused on making flexible capacitors on fabric supports. These electrodes were made using a commercially obtained graphene oxide in water solution, which is diluted with solvent to improve its wetting properties. Once the graphene oxide has been coated onto the fabric, it is either chemically reduced using monohydrate hydrazine or thermally reduced by annealing to produce conductive graphene. The fabrics that have been investigated include carbon fiber, which works well due to its inherent conductivity, and Kevlar, which is not conductive. Unfortunately, a graphene coating on Kevlar is not conductive enough to produce an electrode with sufficiently low resistance. We have, therefore, used Ni-coated Kevlar to achieve adequate conductivity, and we plan to investigate whether the incorporation of CNTs can perform the same function as the nickel. A small amount of added graphene greatly increases the capacitance achieved with these conductive fabrics with a capacitance of ~ 80 F/g of graphene being realized. This represents a first step towards the development of a ballistic protection vest that also is useful for energy storage.

Another approach to flexible graphene-based electrodes has been pursued with Prof. Woo Lee at Stevens Institute of Technology. His group has been developing an inkjet printing approach to flexible graphene electrode fabrication on Kapton films, and together we have demonstrated capacitances of ~ 75 F/g of graphene. The goal of this project is to be able to print entire circuits including energy storage onto flexible substrates, which can be inserted into Armament Research, Development and Engineering Center (ARDEC) munitions.

4.7 Conclusions and Opportunities

In the present work, a systematic comparison of different CNT solution compositions and deposition methods has been undertaken to determine the important factors in electrode fabrication. We have found that it is best to use solutions free from additives that may be difficult to remove from the fabricated electrode. In addition, the CNT solution processing (e.g., dilution and sonication) has a small effect on the resulting specific capacitance as did the

deposition methods used here. In the end, the choice of fabrication method may be determined by other factors such as manufacturability, cost, convenience, uniformity, or the efficiency with which the CNTs are used.

Continuing work will focus on the fundamental capacitance limits, such as quantum capacitance limits, of CNTs/G electrodes to determine if further fabrication method development is warranted. We are currently attempting to address these issues by investigating the quantum capacitance limitations through the fabrication of single layer graphene electrodes.

Even if CNTs/graphene electrodes do not yield specific capacitances in excess of activated carbon, they may still yield improvements in power due to increased electrode conductance. There may also be important supercapacitor improvements due to the mechanical properties of CNTs/graphene. For instance, CNTs/graphene lend themselves to flexible, conformal, or integrated supercapacitors that would be useful for applications where there is little available space. ARL will continue to advance supercapacitor power and energy density through optimizing electrode surface area and porosity coupled with the incorporation of pseudocapacitance. In the final application, a supercapacitor may be part of a hybrid system that couples a load leveling supercapacitor to a battery, fuel cell, energy harvester, or other energy source.

5. Simulation and Modeling

In the first year of the graphene modeling effort, emphasis has been on laying the groundwork for a device simulation program that incorporates the unique features of graphene into a standard package for circuit simulation and device synthesis. With the goal of avoiding large-scale computer simulation except when necessary, the modeling approach has been to graft graphene physics onto traditional analytic device models based on semiconductor properties and classical electrical/fluid dynamic analysis. Results for this year included the following:

- A lengthy ARL technical report (TR) on the gradual-channel modeling of graphene FETs (41) based on current III-V high electron mobility transistor (HEMT) devices, including the low dimensionality and ambipolar character of the charge transport. In this modeling formalism the emphasis is on the drain circuit, with the gate circuit treated in an elementary way. Several types of carrier scattering were included in the transport, and mathematical expressions for the differing current versus voltage (I-V) curves resulting from these scattering assumptions were derived. Simulations with these models reproduced the characteristic features of the transistor transfer characteristics, notably the “kink” in the source-drain I-V curves due to ambipolarity. In addition, the issue of unphysical negative conductance exhibited by the simplest large-signal models was addressed, which is especially problematic for RF equivalent circuit modeling. Figure 13 shows a commonly

used graphene FET structure, equipped with two gates in order to “electrostatically dope” the device either n- or p-type. Figure 14 shows an example of a transistor simulation using one type of gradual-channel model (42). In this figure the transistor drain-source current I_D is plotted versus drain voltage V_{ds} for three values of gate voltage V_{gs} , i.e., transfer characteristics, using transistor parameters given in reference 42. For this simulation a rather low value of 2.5×10^7 cm/s was chosen for the saturation velocity v_{sat} . The simulation predicts negative conductance in the drain circuit for gate voltages exceeding a threshold value of 3.58 V. In figure 14, the blue curve is for a gate voltage below this threshold and shows a kink with positive slope, i.e., the conductance is positive; whereas, the red curve is for a device gated at threshold, where the kink has zero slope, and the yellow curve is for a device gated above threshold, with a region of negative conductance.

The output conductance $s_d = \frac{dI_D}{dV_{ds}}$ and transconductance $g_m = \frac{dI_D}{dV_{gs}}$ are shown in figures 15 and 16; the absolute value of g_m is plotted in accordance with reference 42.

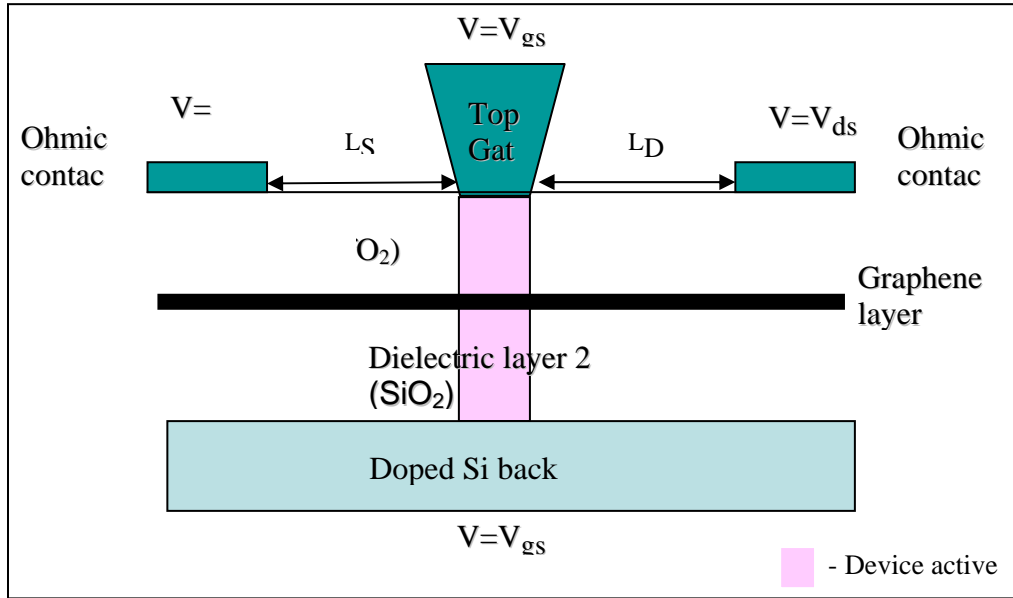


Figure 13. Dual-gate graphene FET structure (42).

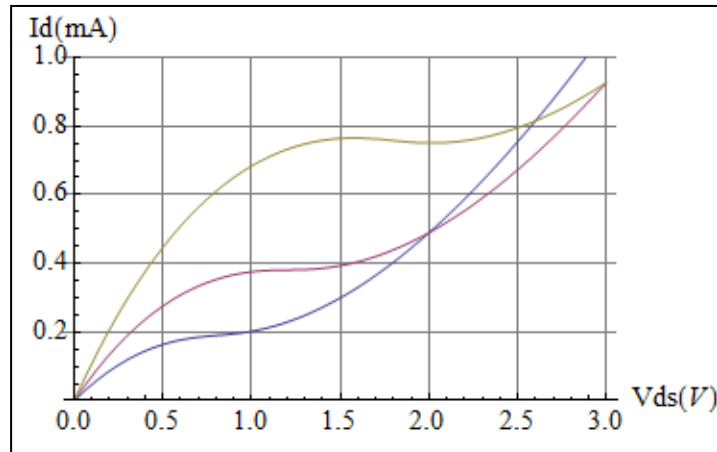


Figure 14. I_d versus V_{ds} for simulator model.

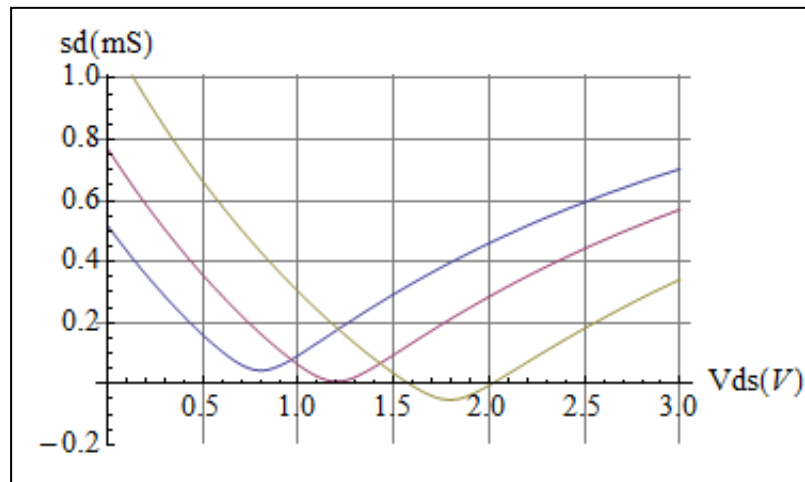


Figure 15. s_d vs. V_{ds} for simulator model.

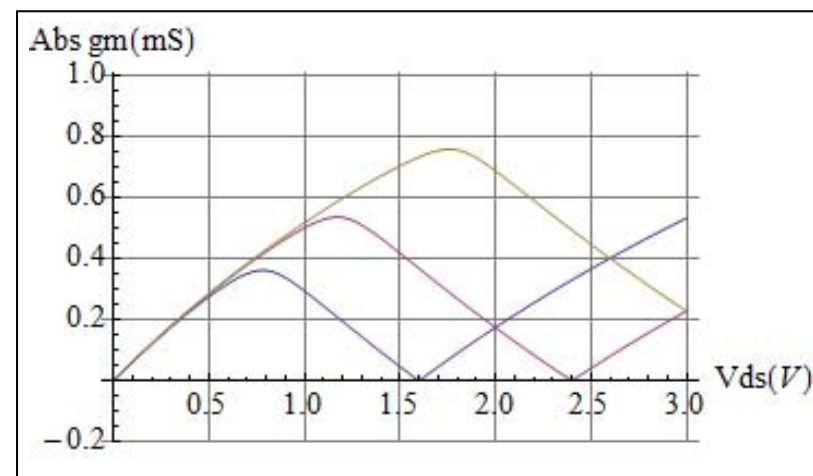


Figure 16. $|g_m|$ versus V_{ds} for simulator model.

A detailed discussion is given in the TR of how to remove negative resistance from the transistor I-V curve. Figure 17 shows the effectiveness of this technique.

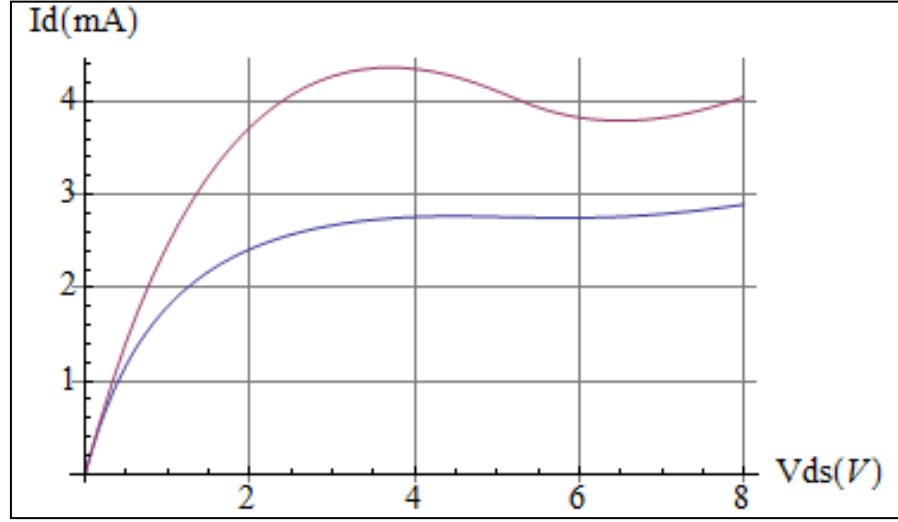


Figure 17. I_d versus V_{ds} for $V_{gst} = 7.58$ V. Red curve – uncorrected model; blue curve – corrected model.

- Development of an RF equivalent circuit, as part of a fitting program to link RF measurements with device electrical and material parameters. The circuit, which is shown in figure 18, includes an RF port representing the back gate included in many transistor device structures. Expressions for the S-parameters of this network were derived and will be used for fitting the experimental numbers and extracting circuit parameters, which will reveal various aspects of the transistor functioning.

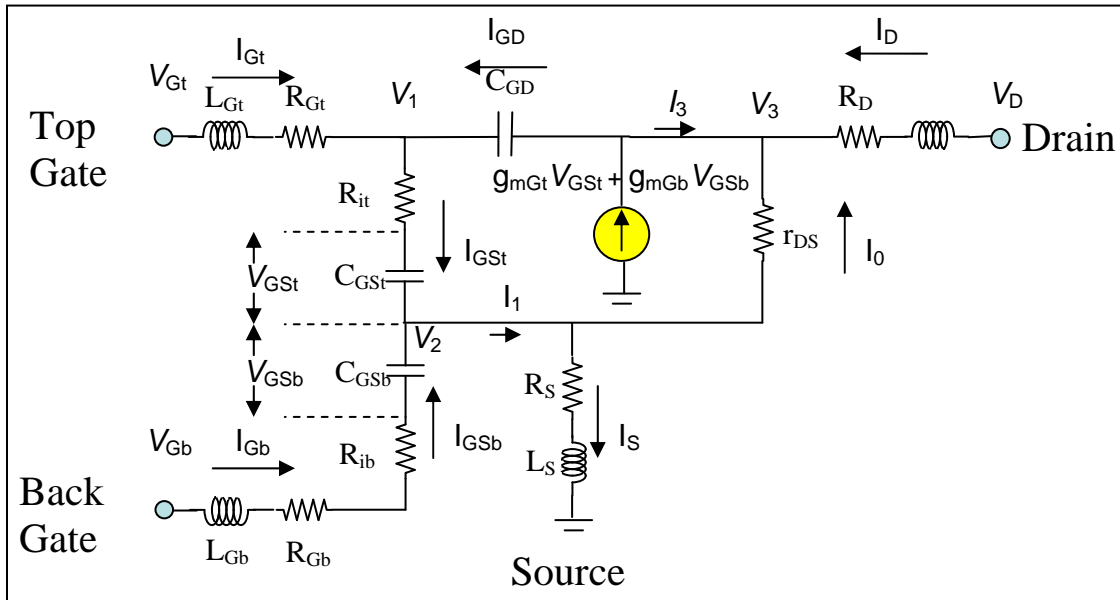


Figure 18. RF equivalent circuit for a double-gate graphene FET.

- A second ARL TR on the modeling of graphene-loaded capacitors/varactors (43). This TR, which is in progress, discusses the simplest model of the graphene FET gate structure: a simple capacitor with a graphene layer sandwiched between two dielectrics, as shown in figure 19 (compare to figure 13).

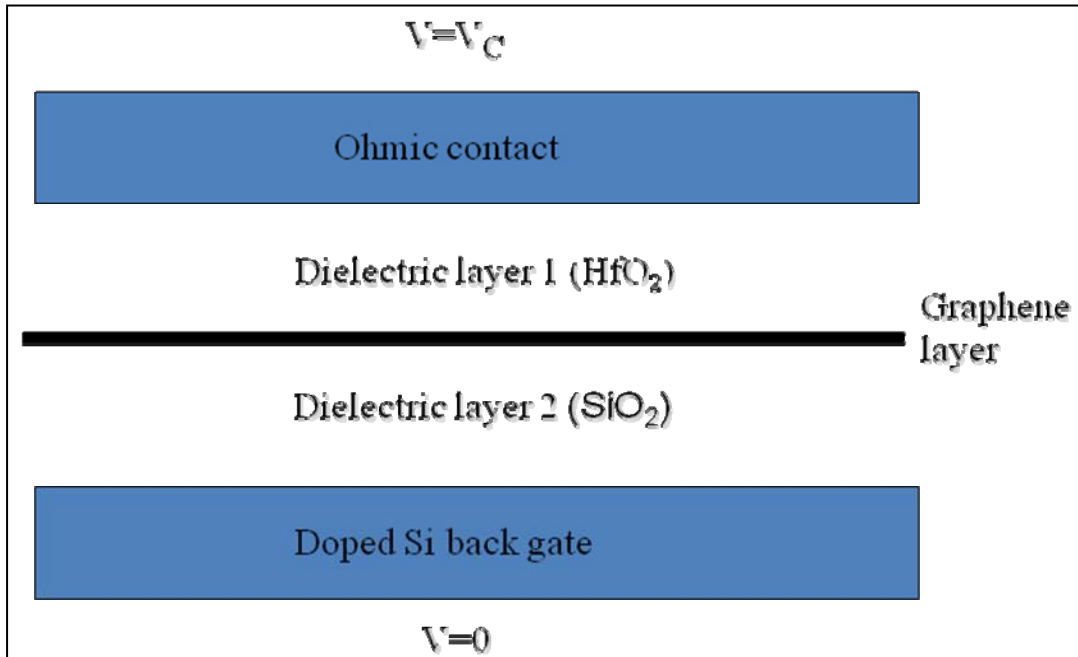


Figure 19. Graphene-loaded capacitor.

Due to its simplicity this structure can be analyzed in great detail, making it possible to replace the empirical voltage of the graphene FET on channel density with a true quantum-mechanical expression. An additional byproduct of this analysis is the possibility of studying the capacitor itself at large signal levels, i.e., treating it as a varactor. Figure 20 shows the second-harmonic response of the graphene varactor to an applied voltage.

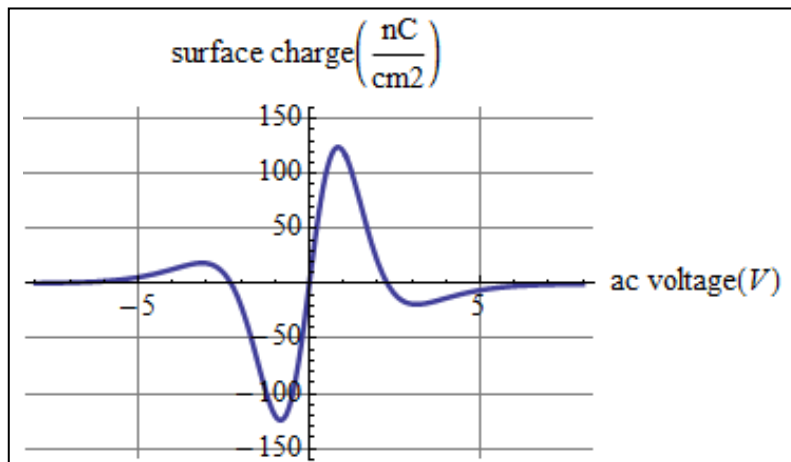


Figure 20. 2nd harmonic surface charge density vs. alternating current (AC) voltage.

The feasibility of using this structure as a varactor will be studied in the coming year.

6. Conclusions

The following tasks were accomplished:

- Designed and constructed two graphene CVD systems: (1) atmospheric pressure and (2) low pressure.
- Developed a CVD process for graphene growth and testing techniques.
- Designed and fabricated novel device structures.
- Established infrastructure for testing and evaluation of graphene transistors and electronics.
- Developed device physics modeling.

6.1 Transitions

Discussion is in progress with CERDEC for communications and Defence Advanced Threat Reduction Agency (DATRA) on sensors applications.

6.2 Future Research

1. G-growth, doping and domain study:
 - Optimize the pressure, temperature, cooling rate, and post annealing under different gases.
 - Mix gases during/after G-growth, optimize transfer process, and selection of substrates: boron nitride (BN) and aluminum nitride (AlN).
 - Optimize catalyst size, orientation, surface smoothness, and grain boundaries.
2. Atomic layer deposition of dielectric contacts:
 - Stabilize and analyze deposition parameters for reliable films deposition
 - Study dielectric behavior for highest possible electrical breakdown device applications
 - Study deposition condition for low resistivity
3. Characterization:
 - Raman spectroscopy for single (S), bi- (B), and multi- (M) layers (L); defects centers and domain boundaries
 - AFM/Raman for focused areas evaluation,

- High-resolution transmission electron microscopy (HRTEM) for defects and domain structures
 - Electrical characterization for doping evaluation
4. Device test structures:
- Develop internal process and fabrication capabilities to prototype device test structures.
 - Develop tech to scale down to nanometer size and device test structures.
 - Design and develop tools setup to study devices electron, holes, and scattering behavior.
5. RF testing:
- Collaborate with RF Branch to measure and evaluate RF performance for specific applications.
6. Modeling:
- Device physics modeling
 - Electronic device modeling
 - Basics of electron, holes, doping, impurities, and scattering centers in G

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List of Symbols, Abbreviations, and Acronyms

0-D	zero-dimensional
1-D	one-dimensional
2-D	two-dimensional
3-D	three-dimensional
AC	alternating current
AFM	atomic force microscopy
Al ₂ O ₃	aluminum oxide
ALC	Adelphi Laboratory Center
ALD	atomic layer deposition
AlN	aluminum nitride
APCVD	atmospheric pressure chemical vapor deposition
Ar	argon
ARDEC	Armament Research, Development and Engineering Center
ARL	U.S. Army Research Laboratory
Au	gold
B	bi-
BN	boron nitride
CERDEC	U.S. Army Communications-Electronics Research, Development and Engineering Center
CH ₄	methane
CMOS	complementary metal-oxide-semiconductor; a technology for constructing integrated circuits
CNT	carbon nanotube
Cr	chromium
CV	cyclic voltammetry

C-V	capacitance-voltage
Cu	copper
CVD	chemical vapor deposition
DATRA	Defence Advanced Threat Reduction Agency
DI	de-ionized
DP	Dirac point
DSI	Director's Strategic Initiative
FET	field-effect transistor
F/g	Farads per gram
FWHM	full-width-at-half-maximum
G	graphene
GFET	graphene field-effect transistor
GO	graphene oxide
H ₂	hydrogen, the diatomic molecule
H ₂ O	water
HEMT	high electron mobility transistor
HOPG	highly ordered pyrolytic graphite
HRTEM	high-resolution transmission electron microscopy
I-V	current versus voltage
IPA	isopropanol
L	layers
LPCVD	low pressure chemical vapor deposition
KOH	potassium hydroxide
M	multi-
MFC	mass flow controller
MIT	Massachusetts Institute of Technology
MLG	multilayer graphene

Ni	nickel
PMMA	poly(methyl methacrylate)
PVA	polyvinyl alcohol
RF	radio frequency
SEM	scanning electron microscopy/graph
S	single
Si	silicon
SiC	silicon carbide
SiO ₂	silicon dioxide
SLG	single layer graphene
Ti	titanium
TMA	trimethylaluminum
TR	technical report

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